Low Earth Orbit Space Environment Testing of Extreme Temperature 6H-SiC JFETs on the International Space Station

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Abstract. This paper reports long-term electrical results from two 6H-SiC junction field effect transistors (JFETs) presently being tested in Low Earth Orbit (LEO) space environment on the outside of the International Space Station (ISS). The JFETs have demonstrated excellent functionality and stability through 4600 hours of LEO space deployment. Observed changes in measured device characteristics tracked changes in measured temperature, consistent with well-known JFET temperature-dependent device physics.

Introduction

NASA is developing very high temperature semiconductor integrated circuits (ICs) based on silicon carbide (SiC) junction field effect transistors (JFETs) for beneficial use in the hot sections of aircraft engines and for future Venus surface exploration missions. Additional applications for electronics that can operate at temperatures greater than 300 °C (i.e., beyond the temperature capability of silicon-on-insulator electronics) include automotive engines and deep-well drilling [1]. The fabrication of 6H-SiC JFETs, IC formation using single-level metal interconnect, and subsequent operation of transistors and simple integrated circuits at 500 °C for thousands of hours have been previously reported [2,3]. In addition to extreme high temperature operating capability, some applications may require functionality in space environment. This paper reports long-term electrical results from two 6H-SiC junction field effect transistors (JFETs) presently being tested in Low Earth Orbit (LEO) space environment on the outside of the International Space Station (ISS).

Experimental

The NASA Glenn JFET chips were selected from the same 6H-SiC wafer as chips that have previously demonstrated stable electrical operation for thousands of hours at +500 °C [2,3]. More recently, integrated circuits from this same wafer were successfully operated across the very broad temperature range of -125 °C to +500 °C without changing supply voltages [4]. For this experimental test on the ISS, one JFET was packaged for flight in a conventional TO-8 package, while another was bonded into a custom ceramic package capable of prolonged 500 °C high temperature (HT) operation [5]. Both 6H-SiC JFETs featured identical gate length L_G = 10μm and gate width W_G = 40 μm dimensions. SiC JFET technology/fabrication issues are discussed in [2,3].

The packaged JFETs were mounted onto a custom-built experimental circuit board designed to autonomously measure and digitize JFET DC drain current-voltage (I-V) characteristics at applied voltage biases up to 15 V. An overview of the design and build-up of this circuit board are presented in [6]. Fig. 1a shows a photo of the completed experimental circuit board with measurement circuitry and the two SiC JFETs. To comply with ISS flight rules, the board resided inside a 20 cm x 10 cm x 4.5 cm box aluminum box with ~ 1 cm diameter vent opening in the cover that facilitated

shaded (no direct sunlight) JFET exposure to the LEO space environment during flight. This circuit box was integrated with power and communications connections into a larger flight box (called a Passive Experiment Container, PEC, shown in space in Fig. 1b) along with other experiments that collectively comprised the Materials on the International Space Station Experiment 7 (MISSE-7). The MISSE-7 PECs were launched into orbit on 16 November 2009 inside the payload bay of Space Shuttle Atlantis as part of the STS-129 mission to ISS. Astronauts installed the MISSE-7 PECs to the outside of the ISS (at location denoted by arrow in Fig. 1c) during the second STS-129 mission spacewalk.

ISS/MISSE-7 mission protocol dictated that the SiC JFET test board was unpowered between autonomous measurement cycles that were triggered somewhat periodically by a central interface/controller circuit that also relayed the digitized I-V data to ISS for downlink. While on average I-V data was recorded roughly once an hour, there were some prolonged periods where JFET measurements were suspended due to other ISS activities. No temperature control was employed, so the device temperature, as measured by a circuit on the same board as the SiC JFETs, varies between 272 K and 302 K according to the natural thermodynamics of that area of the orbiting ISS. As of 2 June 2010, over 5200 measurement cycles on each JFET have been recorded in the 4600 hours since the first on-orbit I-V test commenced on 22 November 2009.

Results

To date the two LEO space-exposed SiC JFETs have demonstrated excellent functionality and stability. Fig. 2 illustrates measured drain current I_D vs. drain voltage V_D I-V characteristics for various gate voltage V_G steps for both JFETs at a benchmark measurement temperature of T =

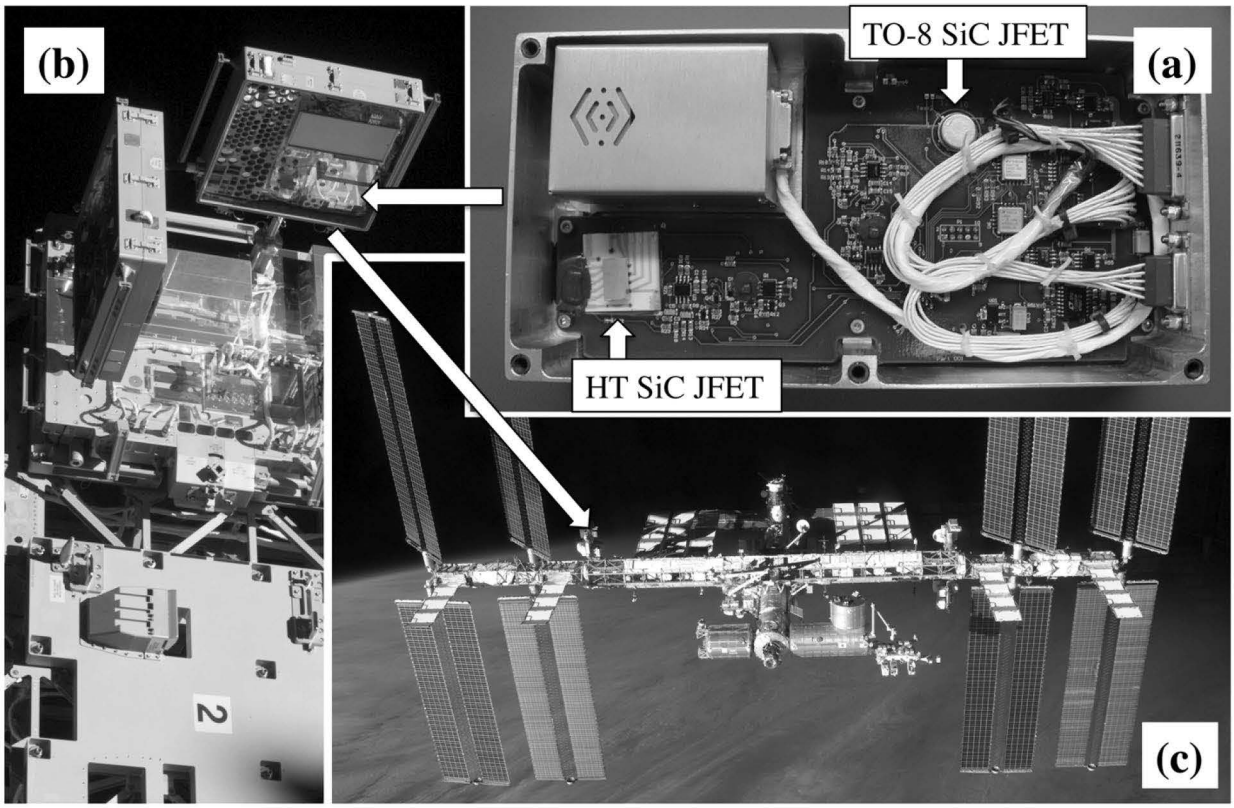

Fig. 1. (a) Custom circuit board with two SiC JFETs mounted for on-orbit I-V measurements. HT SiC JFET resides in a custom ceramic high-temperature package, while the other JFET resides in commercially available TO-8 package. White arrowhead in (b) points to covered SiC JFET circuit box as deployed within larger MISSE-7 Passive Experiment Container (PEC). White arrowhead in (c) denotes the location of MISSE-7 PECs on outside of the ISS.

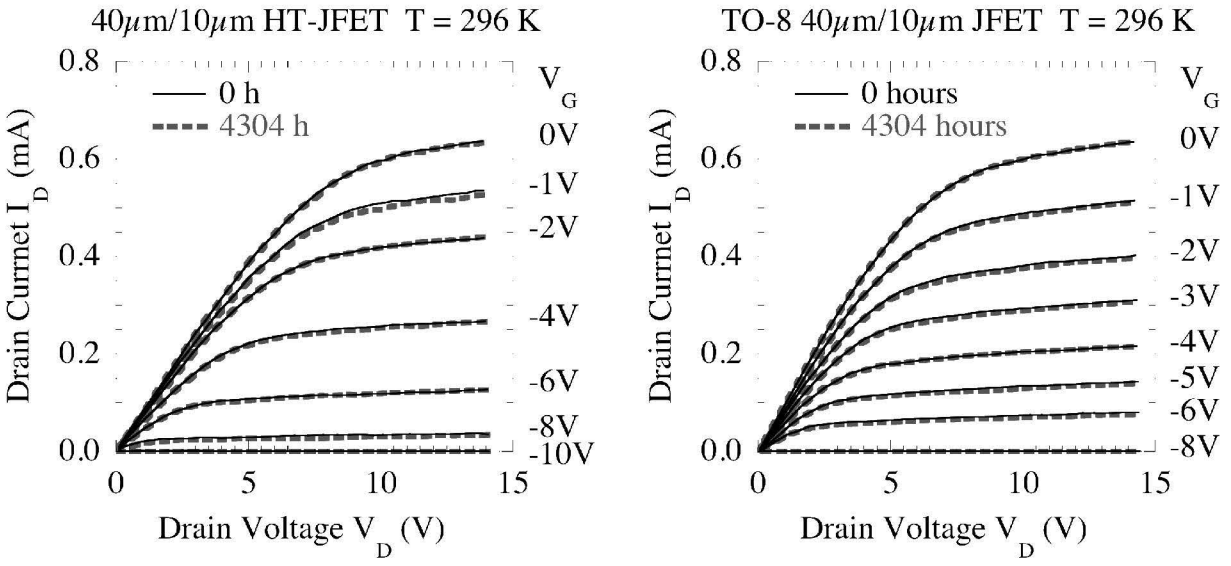

Fig. 2. On-orbit measured drain I-V characteristics of the two SiC JFETs at T = 296 K. The black traces represent the initial I-V measurements recorded following experiment installation on the outside of the ISS, while the dashed grey traces were recorded 4304 hours later.

296 K. The black traces were recorded during the first measurement cycle (time t = 0 hours) while the dashed grey traces were measured 4304 hours later (the last time in the dataset wherein recorded T was 296 K). As illustrated by Fig. 2 data, no significant changes in measured I-V characteristics were observed with time for either device for a given measurement temperature. This same time-invariant behavior is also evident in Fig. 3 plots of $\sqrt{I_D}$ vs. V_G transistor characteristics. The threshold voltage V_T extrapolated from respective x-axis intercepts in Fig. 3 exhibit negligible change between the 0 hours and 4304 hours. The difference in V_T between the two JFETs exists due to epilayer doping/thickness variation across the original 6H-SiC wafer [3]. To within the limitations of the measurement circuit (~1μA current resolution) [6], the ISS SiC JFETs exhibited complete turn-off behavior that did not change with time on orbit for a given temperature.

Fig. 4 summarizes the complete time variation of two key SiC JFET on-state parameters recorded throughout the first 4600 hours of on-orbit testing. In particular, the drain resistance R_{DS} and drain saturation current I_{DSS} (both extracted from the $V_G = 0$ I_D vs. V_D I-V characteristics) are respectively plotted in Fig. 4a and Fig. 4b. Since both of these on-state parameters are known to depend on device temperature, the measured circuit board temperature is also plotted in Fig. 4. The temperature data of Fig. 4 exhibits rapid variation (due to sunlight/shading of the experiment as ISS orbits the Earth every 91 minutes relative to roughly hourly JFET data readings) superimposed on a longer-term (~1400 hour period) larger amplitude temperature cycles. The measured R_{DS} and I_{DSS} data of Fig. 4 exhibit corresponding time-dependent features that indicate temperature change as the dominant mechanism behind the observed changes in JFET on-state properties. The fact that R_{DS} decreases where T increases in Fig. 4a indicates that JFET n-channel conduction is more governed by incomplete carrier ionization than electron mobility for these particular experimental conditions [7]. Consistent with known SiC JFET device physics, I_{DSS} exhibits opposite temperature correlation than

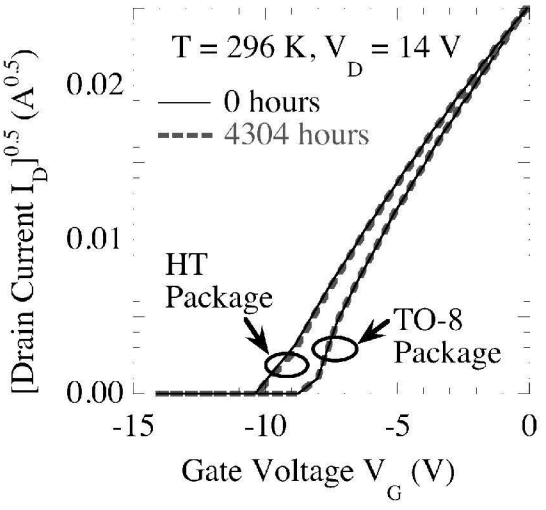

Fig.3. On-orbit measured drain $\sqrt{I_D}$ vs V_G turn-off characteristics of the SiC JFETs.

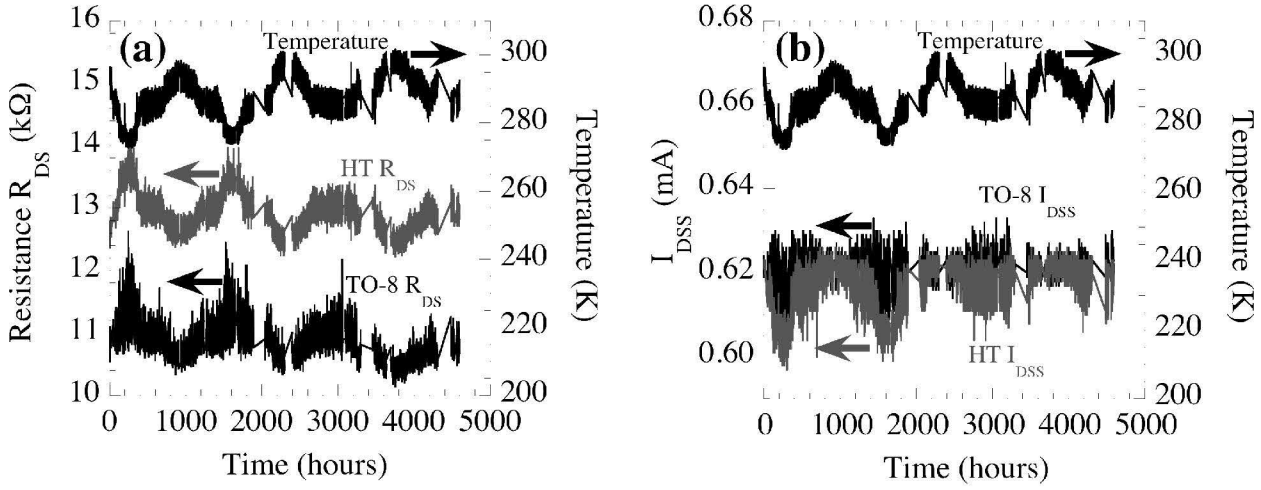

Fig. 4. Plots of measured circuit board temperature and (a) JFET drain resistance R_{DS} and (b) JFET channel saturation current I_{DSS} for both JFETs as a function of on-orbit time.

R_{DS} in that I_{DSS} increases with increasing T. Even with the roughly 30 °K measurement temperature spread, R_{DS} did not change more than 16% while the largest change in I_{DSS} was less than 5%.

Summary Discussion

The extreme temperature SiC JFETs and packaging have successfully operated free of degradation over the 4600 hours of LEO space environment exposure time to date. However, the LEO/ISS space environment is relatively benign compared to 500 °C room air oven tests that NASA GRC chips and packaging have already demonstrated the capability to withstand for thousands of hours in prior ground testing [2,3]. Accounting just for shielding provided by the ~ 1 mm thick walls of the aluminum box, the SiC JFET chips have been exposed to less than 1 kRad(Si) total radiation dose to date [8]. This total radiation dose is orders of magnitude below 100 MRad(Si) dose levels that other 6H-SiC JFETs have withstood without significant degradation in prior work [9]. Also, the vacuum of space near 10-20 °C is arguably a less chemically reactive environment compared to oxidizing 500 °C room air oven environment. Nevertheless, the fact that these SiC devices are successfully operating in LEO space should help pave the way for future testing and use of extreme-environment SiC integrated circuits in future space missions.

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